Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) An instruction controlled data processing device~~, the device~~ comprising:

[[-]] an instruction issue unit ~~(10), having an issue slot (11) for issuing instructions from an instruction set, the instruction issue unit issuing~~ that is configured to issue respective ones of ~~the~~ instructions of program code in successive instruction cycles, the instructions including at least a first type of instruction and a second type of instruction;

a clocking circuit that is configured to clock the instruction cycles;

[[-]] a register file ~~(14)~~ with ~~an~~ a read port and a write port;

[[-]] a ~~group (12)~~ plurality of functional units ~~(20a,b)~~, each functional unit ~~(20a,b)~~ having a control input coupled to the issue unit ~~slot (11)~~, an operand input ~~(22a,b)~~ coupled to the read port and a result output coupled to the write port~~, each functional unit (20a,b) being arranged to respond to instructions from a respective sub-set of the instruction set to which the other functional units (20a,b) do not respond, the instruction set further comprising a combination instruction to which a first and second one of the functional units (20a,b) respond~~; and

[[-]] a control unit ~~(28)~~ coupled to the issue unit ~~slot (11) and responsive to the combination instruction from the instruction set~~, that is configured to route the result output of ~~the~~ a first ~~one of the~~ functional units ~~(20a)~~ to the write port of the register file in response to instructions of the first type, and to the operand input of ~~the~~ a second ~~one of the~~ functional units ~~(20b)~~ during an instruction cycle in response to instructions of the second type;

wherein the clock circuit is configured to vary a rate of clocking the instruction cycles in dependence upon whether a current segment of the program code includes one or more instructions of the second type.

2. (Currently amended) ~~An instruction controlled data processing device according to Claim~~ The processing device of claim 1, organized as a VLIW processor, wherein the issue ~~slot (11) being one of~~ unit includes a plurality of issue slots ~~of the instruction issue unit~~ for issuing a VLIW instruction word ~~that contains the combination instruction as one of its instructions~~, the register file ~~(14)~~ having a plurality of sets of read and write ports, the ~~device comprising respective~~ functional units or groups of functional units each coupled to a respective one of the issue slots and the sets of read and write ports ~~for executing respective instructions from the VLIW instruction word, the first and second one of the functional units in responding to the combination instruction issued in the issue slot in parallel with execution of instructions issued in the same instruction word as the combination instruction~~.

3. (Canceled)

4. (Currently amended) ~~An instruction controlled data processing device according to Claim 3, comprising a clock circuit (16) for clocking the instruction cycles,~~ The processing device of claim 1, wherein the clock circuit ~~(16) having~~ includes a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate ~~within an instruction execution cycle the~~ a latency of instructions of the second type involved in producing a result from the second ~~one of the~~ functional units ~~(20b) in response to an operand applied to the first one of the functional units (20a) also~~ during execution of the ~~combination~~ instruction of the second type within the instruction ~~execution~~ cycle, and a second clock rate that is too fast to accommodate ~~said~~ the latency of instructions of the second type in the instruction cycle, but accommodates latency of instructions of the first type ~~from said sub-sets~~.

5. (Currently amended) ~~An instruction controlled data processing device according to Claim~~ The processing device of claim 1, wherein ~~the instruction issue unit (10) has a further issue slot and the register file (14) has a further read port, the device comprising a further functional unit (40b) having a control input coupled to the further issue slot and an operand input coupled to the further read port,~~ the control unit ~~(28) being arranged~~ is configured to selectively route the result output of a third ~~the further~~ functional unit ~~units (40b)~~ to a further operand input of the second ~~one of the~~ functional unit ~~units (20b)~~ under control of the ~~combination~~ instruction of the second type~~, bypassing the register file (14) under control of the combination instruction~~.

6. (Currently amended) ~~An instruction controlled data processing device according to Claim~~ The processing device of claim 5, ~~programmed with a program that contains~~ wherein the program code includes a VLIW instruction that contains a command for the ~~further~~ third functional unit ~~(40b)~~ and the ~~combination~~ instruction of the second type ~~for the group of functional units (12)~~ for issue in a same instruction cycle.

7. (Currently amended) ~~An instruction controlled data processing device according to Claim~~ The processing device of claim 1, wherein the control unit ~~(28)~~ is arranged to make the second ~~one of the~~ functional unit~~s (20b)~~ respond to the ~~combination~~ instruction of the second type in an instruction execution cycle following an instruction execution cycle in which the first ~~one of the~~ functional unit~~s (20a)~~ responds to the ~~combination~~ instruction of the second type.

8. (Currently amended) ~~An instruction controlled data processing device according to Claim~~ The processing device of claim 7, wherein the result of the first ~~one of the~~ functional unit~~s (20a)~~ is routed without intermediate latching from the first ~~one of the~~ functional unit~~s (20a)~~ to the operand input of the second ~~one of the~~ functional unit~~s (20b)~~.

9. (Canceled)

10. (Currently amended) A method of executing a processing task, comprising:

providing a plurality of functional units,

issuing successive instructions at an instruction cycle rate;

executing those of the instructions that are of a first type each with an individual one of the functional units during one instruction cycle,

executing an instruction that is of a second type with a first and a second one of the functional units in series during one instruction cycle;

routing a result of the first one of the functional units to an operand of the second one of the functional units in response to the instruction of the second type; and ~~according to Claim 9, wherein the first and the second one of the functional units (20a,b) respond to the instruction of the second type in a same instruction execution cycle, the method comprising~~

[[-]] selecting ~~an~~ the instruction cycle rate from at least a first and second rate, based on the type of instruction, the first rate being so slow that execution of ~~a combination~~ instructions of the second type by a cascade of at least two of the functional units ~~(20a,b)~~ fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions of the first type ~~by single ones of the functional units~~ fits within the instruction ~~execution~~ cycle at the second rate, execution of ~~the combination~~ instructions of the second type not fitting within one instruction ~~execution~~ cycle at the second rate~~;~~

~~[[-]] adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the combination instruction is used when the task is executed at the first rate and the combination instruction is replaced by instructions of the first type with corresponding effect when the task is executed at the second rate~~.

11. (Currently amended) ~~A method according to Claim 9, comprising~~ The method of claim 10, including

[[-]] issuing the successive instructions each as part of a VLIW instruction word that contains a plurality of instructions for respective further functional units ~~(40a,b)~~;

[[-]] including in the instruction word that contains the instruction of the second type ~~an~~ a further instruction for a particular one of the further functional units ~~(40a,b)~~; and

[[-]] routing a further result of the further instruction from the particular one of the further functional units ~~(40a,b)~~ to a further operand input of the second one of the functional units ~~(20b)~~ in response to the instruction of the second type.

12. (New) The method of claim 10, including adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the instructions of the second type are used when the task is executed at the first rate and the instructions of the second type are replaced by instructions of the first type with corresponding effect when the task is executed at the second rate